

Phone 949-721-1182  
Fax 949-760-9532  
Email:  
mrernieb@ernieslaw.com



Ernest A. Beutler  
Attorney at Law  
A Professional Corporation  
10 Rue Marseille  
Newport Beach, CA 92660

Intellectual Property Law

C of C

100638469

October 31, 2004

**Certificate  
NOV 08 2004  
of Correction**

Commissioner for Patents  
Alexandria, VA 22313

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelop addressed to: Commissioner for Patents, Alexandria on:

October 31, 2004

\_\_\_\_\_  
Date

Ernest A. Beutler, Reg. No. 19901

Re: Title: **INSPECTION METHOD AND  
INSPECTION APPARATUS FOR SEMICONDUCTOR  
CIRCUIT**

Letters Patent No. **6809532 B2**

Issued: **10/26/2004**

Our Reference: **SIMTEK6349**

Dear Sir:

Enclosed for filing is a Certificate of Correction in duplicate in connection with the above-identified patent.

The errors were made by the entry of a proposed amendment after Final Rejection which was refused entry and was withdrawn. As the errors cited in the Certificate of Correction were incurred through the fault of the Patent Office, no fee is believed to be required.

Respectfully submitted,

Ernest A. Beutler  
Registration No. 19901

Enclosures

NOV 12 2004

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,809,532 *B2*

DATED : October 26, 2004

INVENTOR(S) : Chihiro Araki

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1 should read as follows: 1. An inspection method for a semiconductor circuit with a plurality of connected semiconductor devices comprising the steps of applying an electrical load on the circuit, taking a photograph of the circuit with a thermographic camera to detect heat development of each semiconductor device in response to the applied load, and processing the photograph to determine the temperature of the semiconductor devices for determining the quality of circuit and semiconductor devices based on the heat development.

Claim 4 should read as follows: 4. An inspection apparatus for a workpiece consisting of a semiconductor circuit with a plurality of connected semiconductor comprising an apparatus body on which a workpiece to be inspected is set, a loading circuit for applying load corresponding to the condition of use to the workpiece, a power source for supplying a working current to the workpiece through said loading circuit, a (continued on next page)

MAILING ADDRESS OF SENDER:

Ernest A Beutler, Attorney at Law  
 10 Rue Marseille  
 Newport Beach, CA 92660

PATENT NO. 6,809,532

No. of additional copies

→ 1

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NOV 12 2004

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INVENTOR(S) : Chihiro Araki

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Claim 4 continued

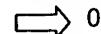
drive waveform generating circuit for applying a drive signal to said workpiece, a thermographic camera for taking photographs of the workpiece set on said apparatus body, an image processor connected to said thermographic camera for determining the temperatures of said semiconductor devices solely from the output of said thermographic camera, and a control for controlling said inspection apparatus to perform an inspection program.

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